

4-Output Part

Overview

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Part: Si5338
 Created By: ClockBuilder Pro v4.4 [2022-03-30]
 Timestamp: 2023-07-25 12:07:57 GMT-06:00

Design Rule Check

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Errors:

- No errors

Warnings:

- No warnings

Design

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Universal Hardware Input Pins:

P3: CLKIN

P4: FDBK

Inputs:

IN3: 25 MHz Single-Ended

Outputs:

CLK0: 25 MHz LVCMOS Single (+) 1.8 V (Buffer)

CLK1: 125 MHz LVDS 1.8 V

CLK2: Unused

CLK3: Unused

Lowest jitter output: CLK1

Device Pinout

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Pin #	Description
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1	CLKIN/XA
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2	CLKINB/XB
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3	CLKIN
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4	FDBK
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5	FDBK
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6	FDBKB
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7	VDD
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8	INTR
---	------

9	CLK3B
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10	CLK3A
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11	VDDO3
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12	SCL
----	-----

13	CLK2B
----	-------

14	CLK2A
----	-------

15	VDDO2
----	-------

16	VDDO1
----	-------

17	CLK1B
----	-------

18	CLK1A
----	-------

19	SDA
----	-----

20	VDDO0
----	-------

21	CLK0B
----	-------

22	CLK0A
----	-------

23	GND
----	-----

24	VDD
----	-----

PAD	GND (Must be grounded for proper device operation)
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Frequency Plan

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Fpfd = 25 MHz
Fvco = 2.5 GHz

P dividers:

P0 = 1
P1 = Unused

M = 100

N dividers:

N0:
Unused

N1:
Value: 20
CLK1: 125 MHz, Error: 0 ppm

N2:
Unused

N3:
Unused

R dividers:

R0 = Unused
R1 = 1
R2 = Unused
R3 = Unused

This datasheet addendum is provided as supplemental information to the Si5338X datasheet, located at www.skyworksinc.com/timing. You can search for and download any datasheet addendum for ClockBuilder Pro generated custom part numbers. Go to <http://www.skyworksinc.com/custom-timing> for more information.

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