

Interfacing TE0715 with TEF0008

Below are listed **MGT** bank reference clock sources.

Clock signal	Bank	Source	FPGA Pin	Notes
MGT _CLK0_P	112	B2B, JM3-33	MGT REFCLK0P_112, U9	Supplied by the carrier board.
MGT _CLK0_N	112	B2B, JM3-31	MGT REFCLK0N_112, V9	Supplied by the carrier board.
MGT _CLK1_P	112	U10, CLK2A	MGT REFCLK1P_112, U5	On-board Si5338A .
MGT _CLK1_N	112	U10, CLK2B	MGT REFCLK1N_112, V5	On-board Si5338A .

Table 5: **MGT** reference clock sources.

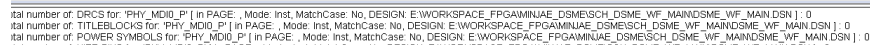
Programmable Clock Generator

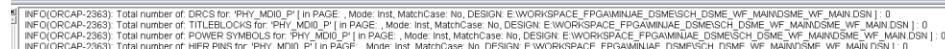
There is a Silicon Labs programmable clock generator Si5338A (U10) chip on the module. It's output frequencies can be programmed via the I²C bus, slave device address is 0x70.

U10 Signal	Default Frequency	Notes
IN1/IN2	Externally supplied	Needs decoupling on carrier board.
IN3	25.000000 MHz	Reference input clock.
IN4	-	Wired to the GND.
IN5/IN6	125 MHz	Ethernet PHY output clock.
CLK0 A/B	-	Not used, disabled.
CLK1 A/B	-	Not used, disabled.
<u>CLK2 A/B</u>	<u>125 MHz</u>	MGT reference clock 1.
CLK3A	-	Bank 34 clock input, default disabled, user clock.
CLK3B	-	Not used, disabled.

Table 12: Programmable clock generator I/Os.

For SFP port, there are 4 ports in the TEF0008 module.
I considered only the first port **SFPA**







CLK2 A/B	125 MHz	MGT reference clock 1.
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