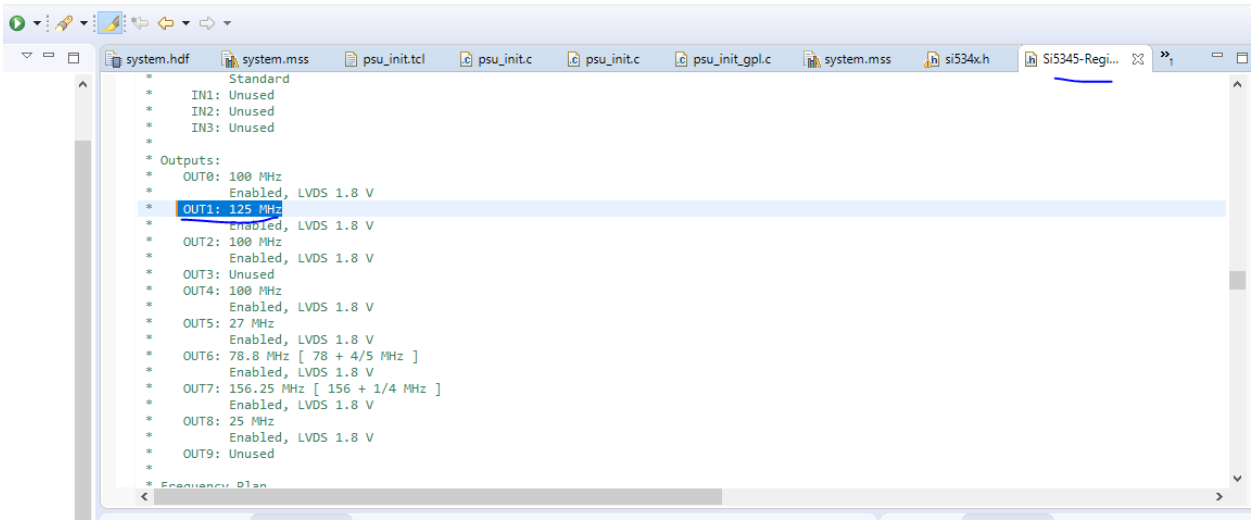
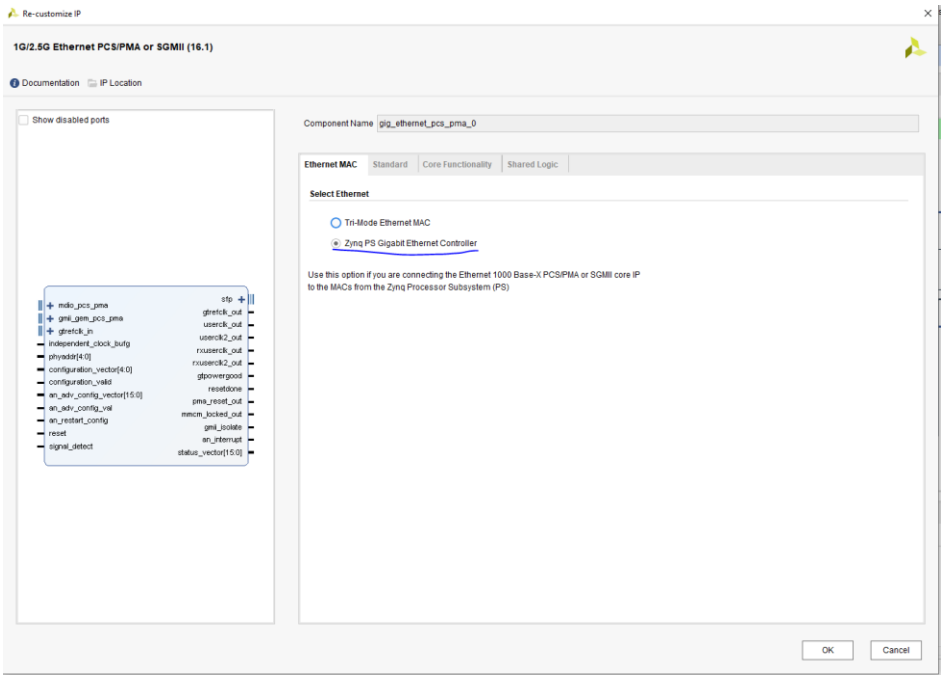
For the differential clock of the GT, I used the differential clock of the board as show in the schematic. I used SFP+ of MGT Lane 2 (B230_RX2_P, B230_RX2_N, B230_TX2_P, B230_TX2_N).

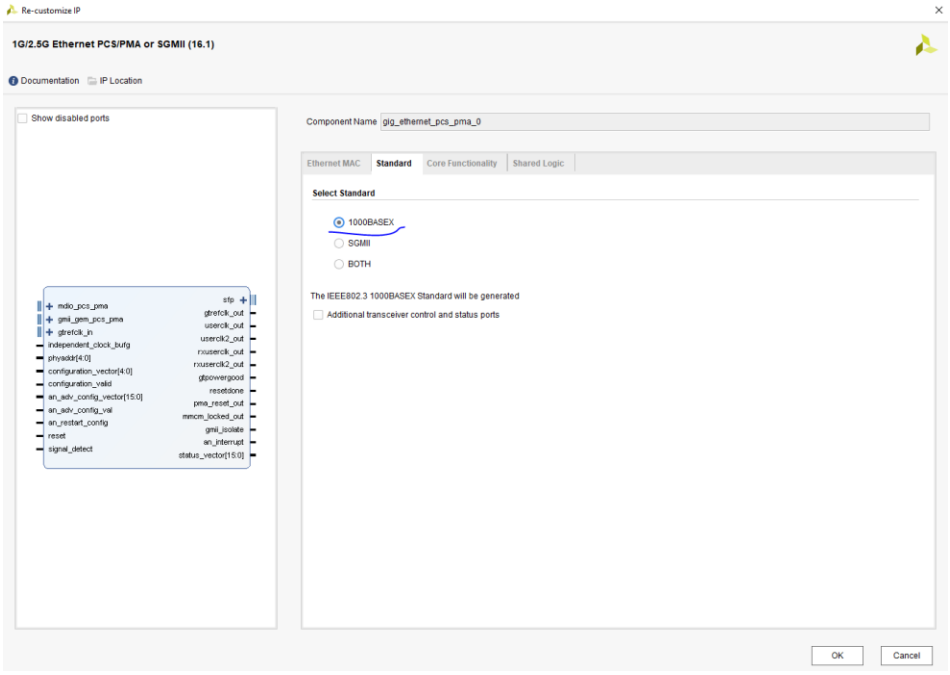
I used the provided SDK-FSBL from TRENZ (TE modified) for programming SI53545.

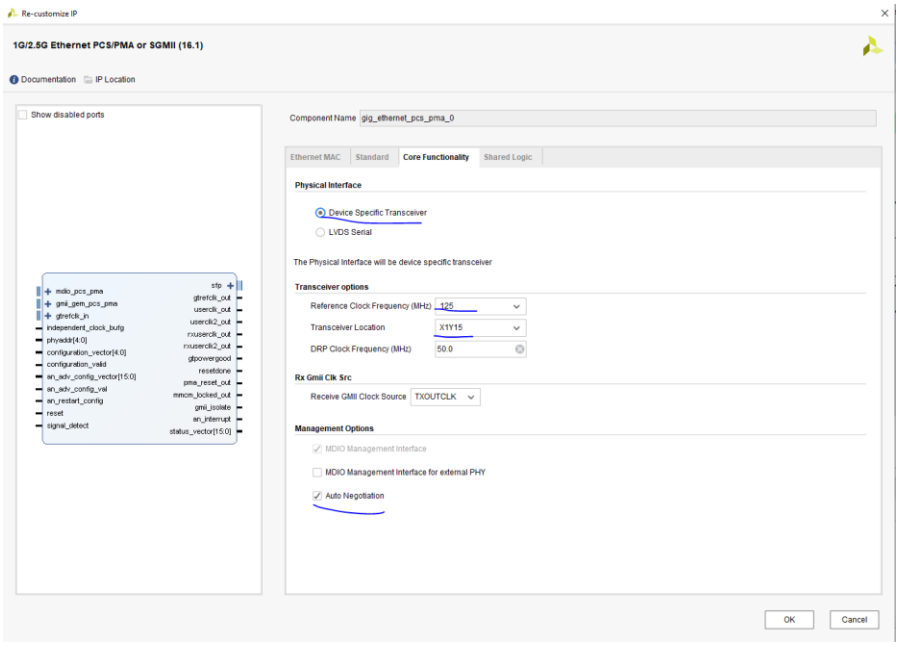
I checked which pins I used to provide clocks to the GT blocks which as follow (Correct me if I am wrong):
Starting from SI53545 --> (OUT1-PIN 28 (CLK1_P)/OUT1B -PIN27 (CLK1_N)) generates 125MHz (based on the SDK TE modified FSBL) --> goes to (B230_CLK0_P and B230_CLK0_N) --> goes to G8 (MGTREFCLK0P_230) and G7 (MGTREFCLK0N_230)

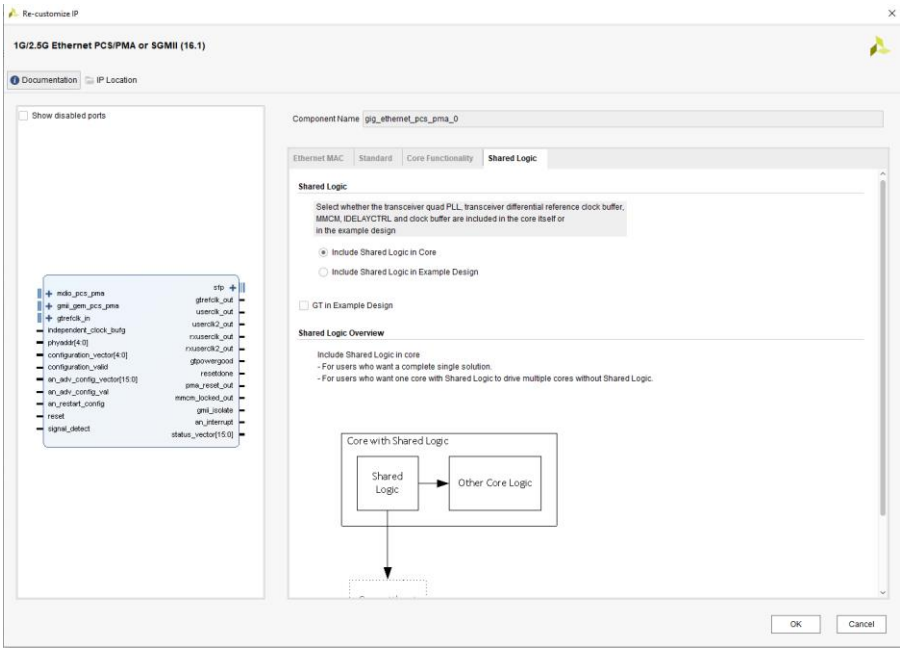


The 1G/2.5G PCS/PMA/SGMII IP block configurations:

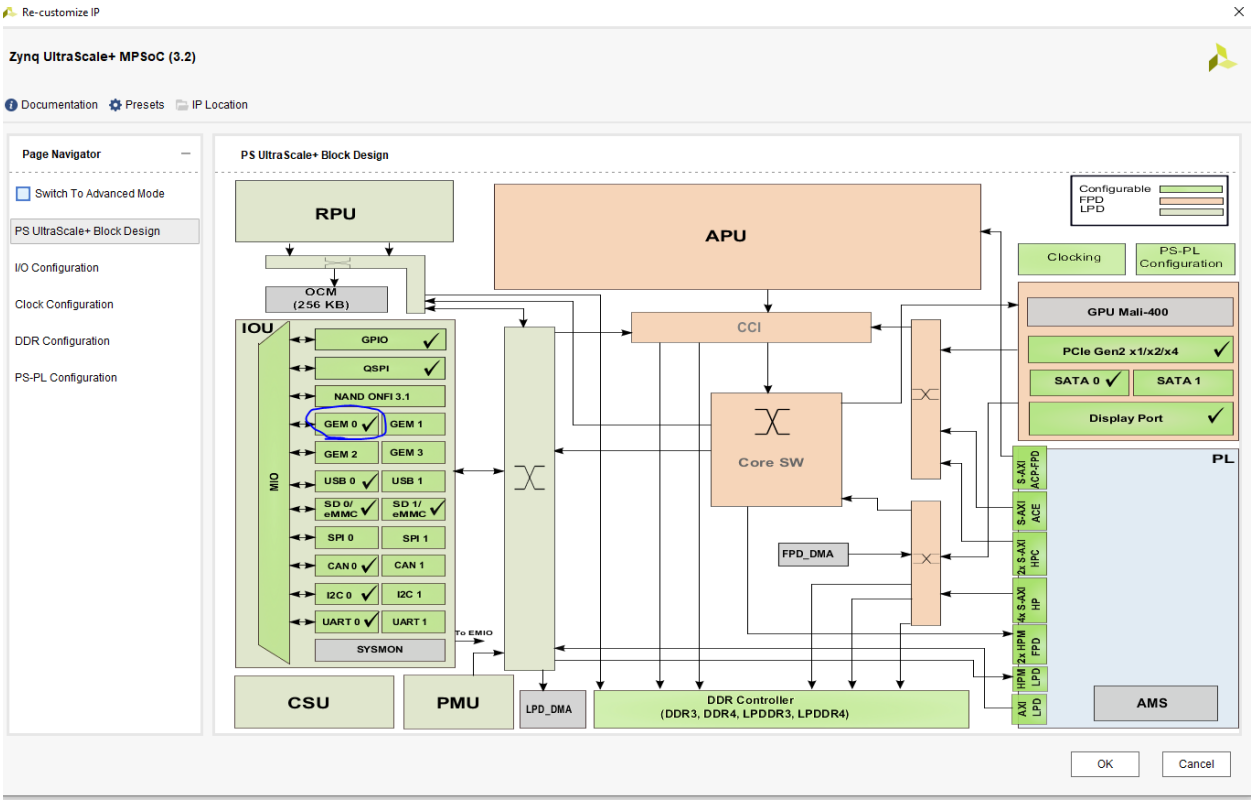


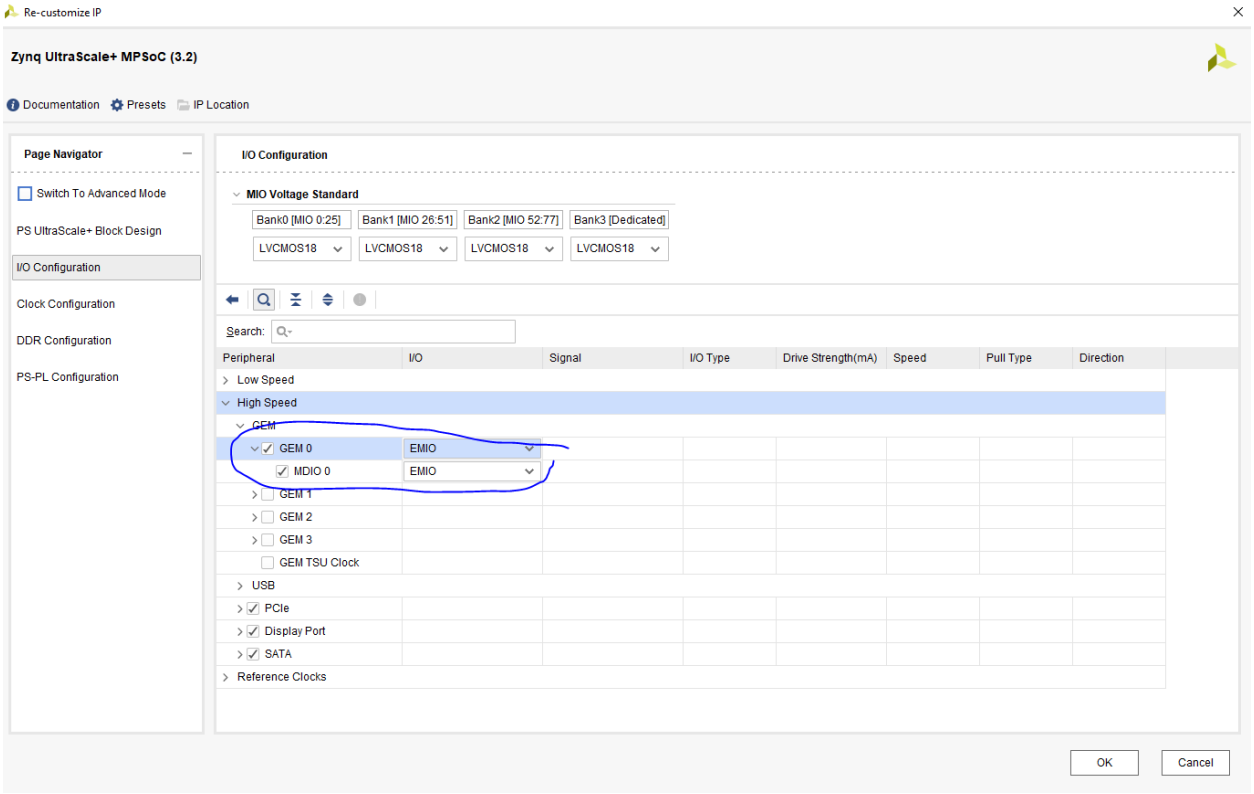

Re-customize IP
1G/2.5G Ethernet PCS/PMA or SGMII (16.1)
Documentation
IP Location
Show disabled ports
Component Name
gig_ethernet_pcs_pma_0
Ethernet MAC
Standard
Core Functionality
Shared Logic
Select Standard
1000BASEX
SGMII
BOTH
The IEEE802.3 1000BASEX Standard will be generated
Additional transceiver control and status ports
mdio_pcs_pma
gmii_gem_pcs_pma
gtrefclk_in
independent_clock_bufg
phyaddr[4:0]
configuration_vector[4:0]
configuration_valid
an_adv_config_vector[15:0]
an_adv_config_val
an_restart_config
reset
signal_detect
sfp
gtrefclk_out
userclk_out
userclk2_out
rxuserclk_out
rxuserclk2_out
gtpowergood
resetdone
pma_reset_out
mmcm_locked_out
gmii_isolate
an_interrupt
status_vector[15:0]
OK
Cancel


Re-customize IP
1G/2.5G Ethernet PCS/PMA or SGMII (16.1)
Documentation
IP Location
Show disabled ports
Component Name
gig_ethernet_pcs_pma_0
Ethernet MAC
Standard
Core Functionality
Shared Logic
Physical Interface
Device Specific Transceiver
LVDS Serial
The Physical Interface will be device specific transceiver
Transceiver options
Reference Clock Frequency (MHz)
125
Transceiver Location
X1Y15
DRP Clock Frequency (MHz)
50.0
Rx Gmii Clk Src
Receive GMII Clock Source
TXOUTCLK
Management Options
MDIO Management Interface
MDIO Management Interface for external PHY
Auto Negotiation
mdio_pcs_pma
gmii_gem_pcs_pma
gtrefclk_in
independent_clock_bufg
phyaddr[4:0]
configuration_vector[4:0]
configuration_valid
an_adv_config_vector[15:0]
an_adv_config_val
an_restart_config
reset
signal_detect
sfp
gtrefclk_out
userclk_out
userclk2_out
rxuserclk_out
rxuserclk2_out
gtpowergood
resetdone
pma_reset_out
mmcm_locked_out
gmii_isolate
an_interrupt
status_vector[15:0]
OK
Cancel

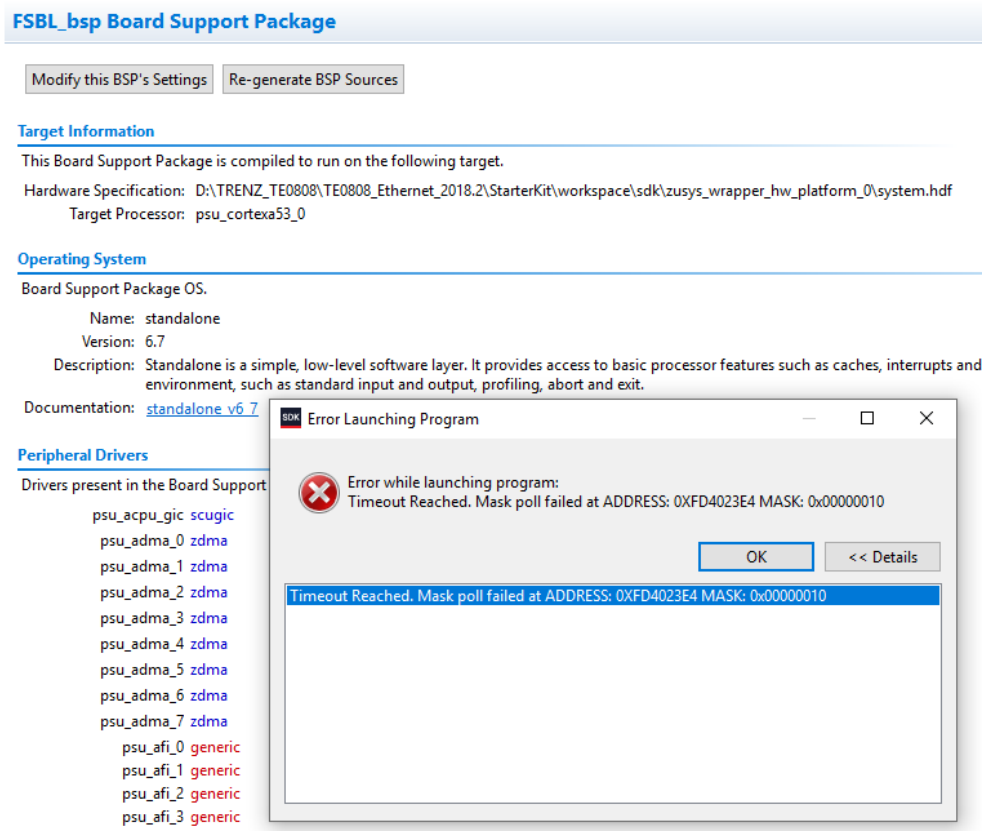


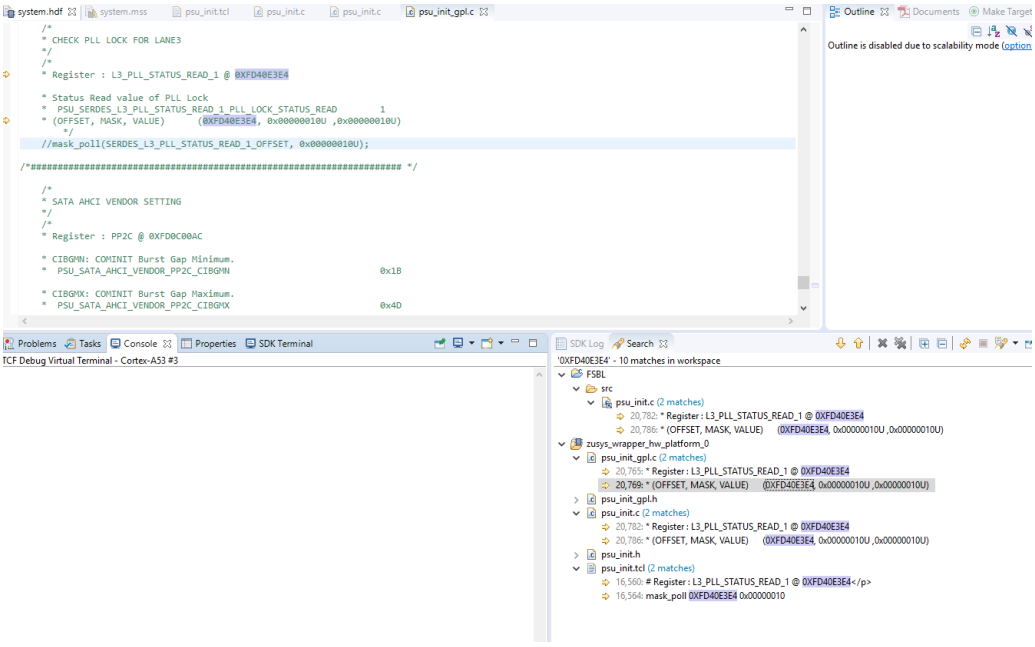
For EMAC I used GEM0





In SDK I fixed the following errors of the FSBL by commenting the corresponding line:





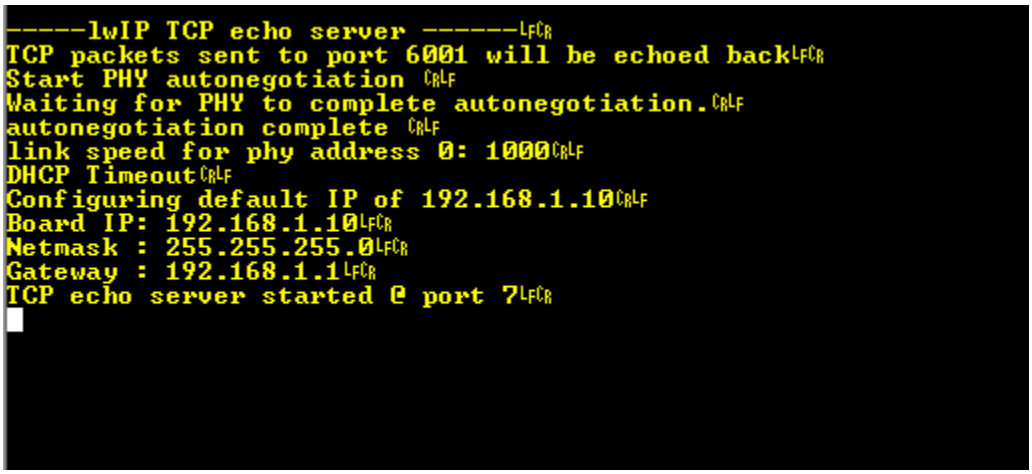
Then I get the following:

```
Xilinx Zynq MP First Stage Boot Loader (TE modified)
Release 2018.2   Jan  9 2020  -  09:28:41
Reset Mode      :      System Reset
Platform: Silicon (4.0), Cluster ID 0x80000000
Running on A53-0 (64-bit) Processor, Device Name: XCZU15EG

--------------------------------------------------------------------------------

TE0808 Board Initialisation
Si534x Init Function
Si534x Init Complete
PCIe Reset Complete

--------------------------------------------------------------------------------

Processor Initialization Done
================== In Stage 2 ============
QSPI 32 bit Boot Mode
QSPI is in Dual Parallel connection
QSPI is using 4 bit bus
FlashID=0x20 0xBB 0x20
MICRON 512M Bits
Multiboot Reg : 0x4000
QSPI Reading Src 0x20000000, Dest FFFF1C40, Length EC0
XFSBL_ERROR_QSPI_LENGTH
Device Copy Failed
Boot Device Initialization failed 0x19
================== In Stage Err ============
Fsbl Error Status: 0x0
```

Using Lwip sometimes I get the following:

```
-----lwIP TCP echo server ------
TCP packets sent to port 6001 will be echoed back
Start PHY autonegotiation
Waiting for PHY to  complete autonegotiation
```

Or



Even when I remove the SFP connector from the cage. !!!!