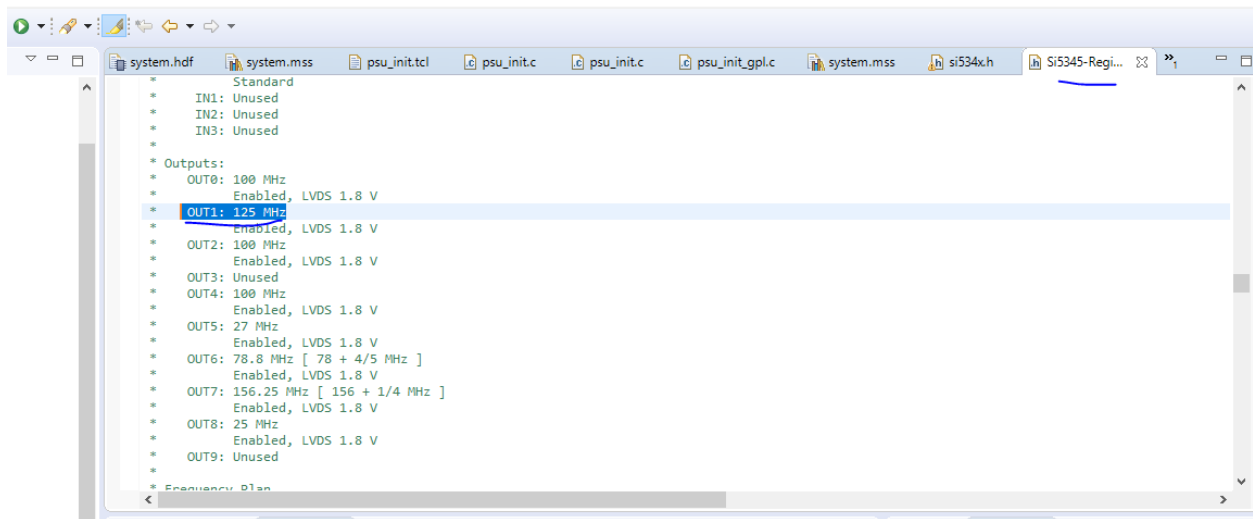


For the differential clock of the GT, I used the differential clock of the board as show in the schematic. I used SFP+ of MGT Lane 2 (B230_RX2_P, B230_RX2_N, B230_TX2_P, B230_TX2_N).

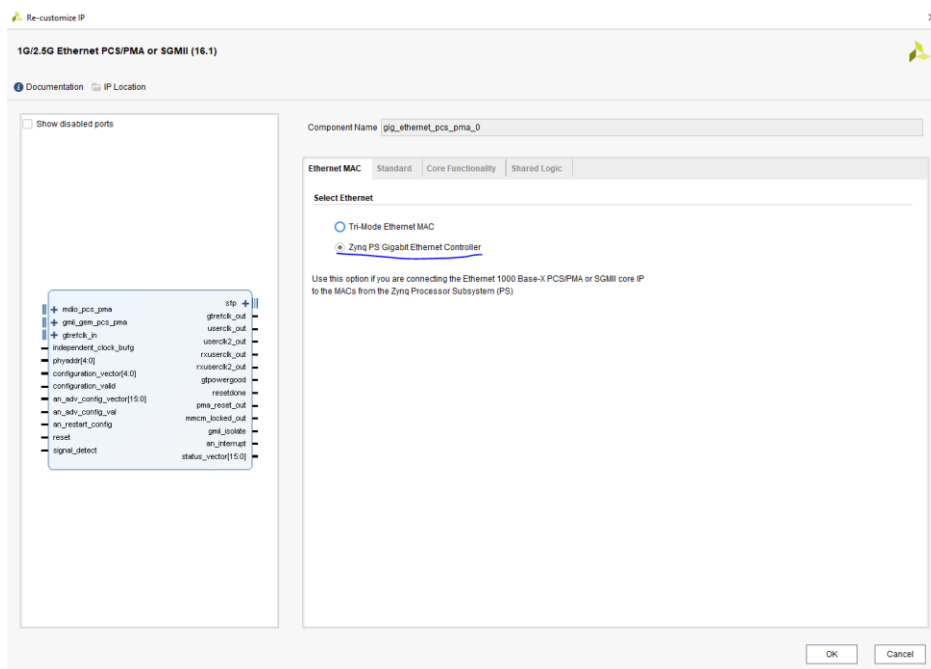
I used the provided SDK-FSBL from TRENZ (TE modified) for programming SI53545.

I checked which pins I used to provide clocks to the GT blocks which as follow (Correct me if I am wrong):

Starting from SI53545 --> (OUT1-PIN 28 (CLK1_P)/OUT1B -PIN27 (CLK1_N)) generates 125MHz (based on the SDK TE modified FSBL) --> goes to (B230_CLK0_P and B230_CLK0_N) --> goes to G8 (MGTREFCLK0P_230) and G7 (MGTREFCLK0N_230)



The 1G/2.5G PCS/PMA/SGMII IP block configurations:



Re-customize IP

10/2.5G Ethernet PCS/PMA or SGMII (16.1)

DocumentationIP Location

Show disabled ports

mdio_pcs_pma

gmii_gmii_pcs_pma

gtrfclk_in

independent_clock_busy

physadd[4:0]

configuration_vector[4:0]

configuration_valid

an_wch_config_vector[15:0]

an_wch_config_val

an_restart_config

reset

signal_detect

stp

gtrfclk_out

userclk_out

userclk2_out

rxuserclk_out

rxuserclk2_out

gtpowergood

resetdone

pma_reset_out

mmcm_locked_out

gmii_locked

an_interrupt

status_vector[15:0]

Component Name

gig_ethernet_pcs_pma_0

Ethernet MAC

Standard

Core Functionality

Shared Logic

Select Standard

1000BASEX

SGMII

BOTH

The IEEE802.3 1000BASEX Standard will be generated

Additional transceiver control and status ports

OK

Cancel

Re-customize IP

10/2.5G Ethernet PCS/PMA or SGMII (16.1)

DocumentationIP Location

Show disabled ports

mdio_pcs_pma

gmii_gmii_pcs_pma

gtrfclk_in

independent_clock_busy

physadd[4:0]

configuration_vector[4:0]

configuration_valid

an_wch_config_vector[15:0]

an_wch_config_val

an_restart_config

reset

signal_detect

stp

gtrfclk_out

userclk_out

userclk2_out

rxuserclk_out

rxuserclk2_out

gtpowergood

resetdone

pma_reset_out

mmcm_locked_out

gmii_locked

an_interrupt

status_vector[15:0]

Component Name

gig_ethernet_pcs_pma_0

Ethernet MAC

Standard

Core Functionality

Shared Logic

Physical Interface

Device Specific Transceiver

LVDS Serial

The Physical Interface will be device specific transceiver

Transceiver options

Reference Clock Frequency (MHz)125

Transceiver LocationX1Y15

DRP Clock Frequency (MHz)50.0

Rx Gmii Clk Src

Receive Gmii Clock SourceTXOUTCLK

Management Options

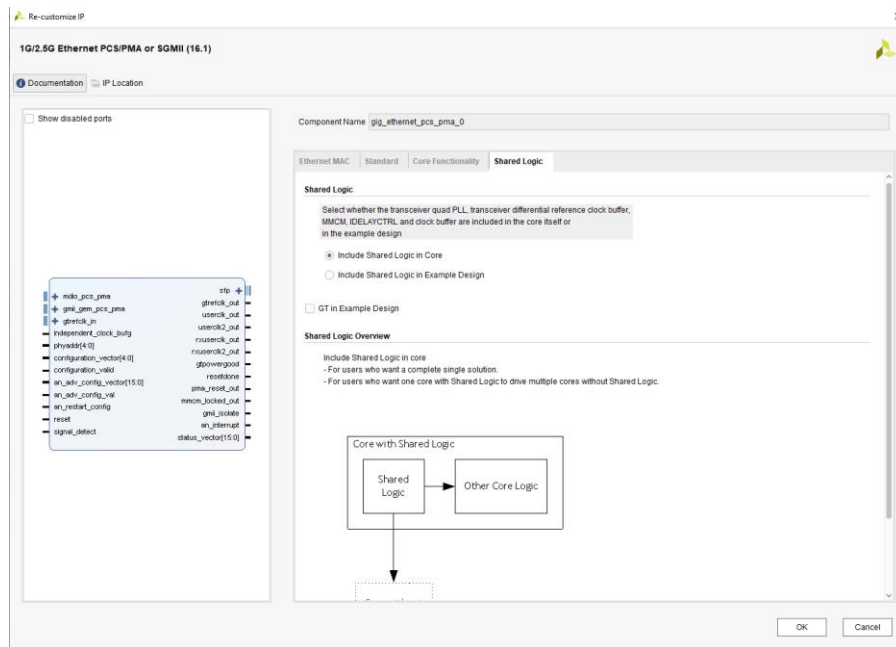
MIO Management Interface

MIO Management Interface for external PHY

Auto Negotiation

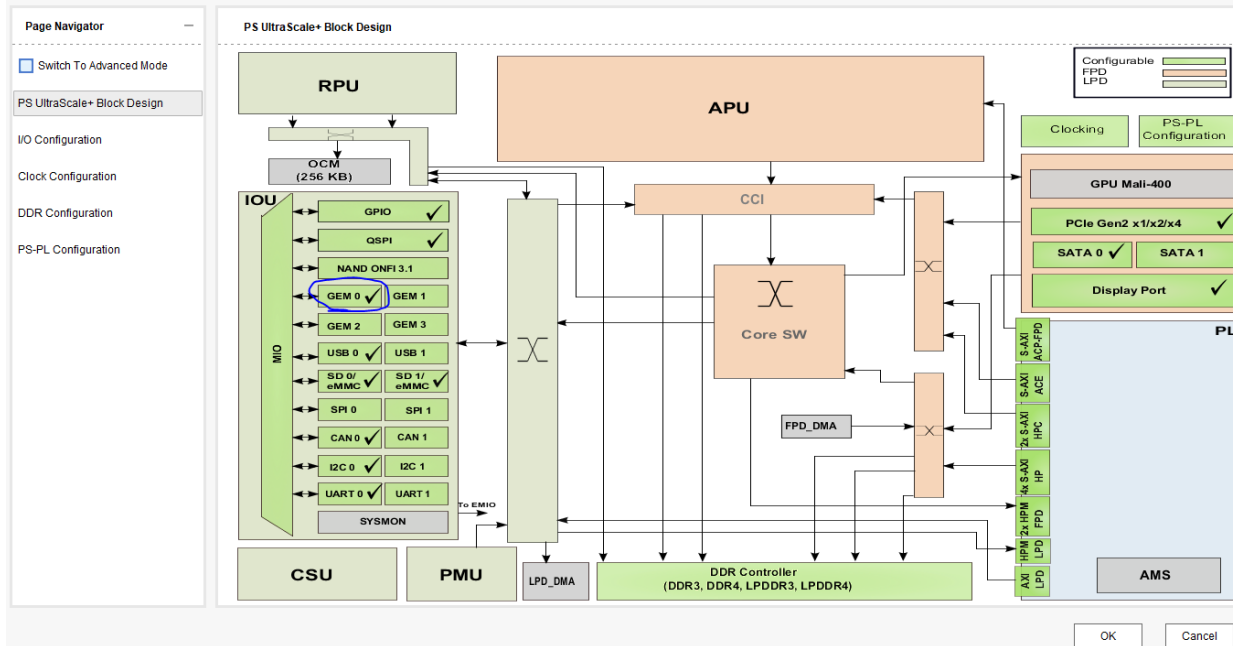
OK

Cancel



For EMAC I used GEM0

Zynq UltraScale+ MPSoC (3.2)


[Documentation](#) [Presets](#) [IP Location](#)


Zynq UltraScale+ MPSoC (3.2)


[Documentation](#) [Presets](#) [IP Location](#)

Page Navigator

- ☐ Switch To Advanced Mode
- PS UltraScale+ Block Design
- I/O Configuration
- Clock Configuration
- DDR Configuration
- PS-PL Configuration

I/O Configuration

MIO Voltage Standard

Bank0 [MIO 0:25] Bank1 [MIO 26:51] Bank2 [MIO 52:77] Bank3 [Dedicated]

LVC MOS18 LVC MOS18 LVC MOS18 LVC MOS18

Search:

Peripheral	I/O	Signal	I/O Type	Drive Strength(mA)	Speed	Pull Type	Direction
Low Speed							
High Speed							
GEM							
<input checked="" type="checkbox"/> GEM 0	EMIO						
<input checked="" type="checkbox"/> MDIO 0	EMIO						
GEM 1							
GEM 2							
GEM 3							
GEM TSU Clock							
USB							
PCIe							
Display Port							
SATA							
Reference Clocks							

OK Cancel

In SDK I fixed the following errors of the FSBL by commenting the corresponding line:

FSBL_bsp Board Support Package

Modify this BSP's Settings

Re-generate BSP Sources

Target Information

This Board Support Package is compiled to run on the following target.

Hardware Specification: D:\TRENZ_TE0808\TE0808_Ethernet_2018.2\StarterKit\workspace\sdk\zusys_wrapper_hw_platform_0\system.hdf

Target Processor: psu_cortexa53_0

Operating System

Board Support Package OS.

Name: standalone

Version: 6.7

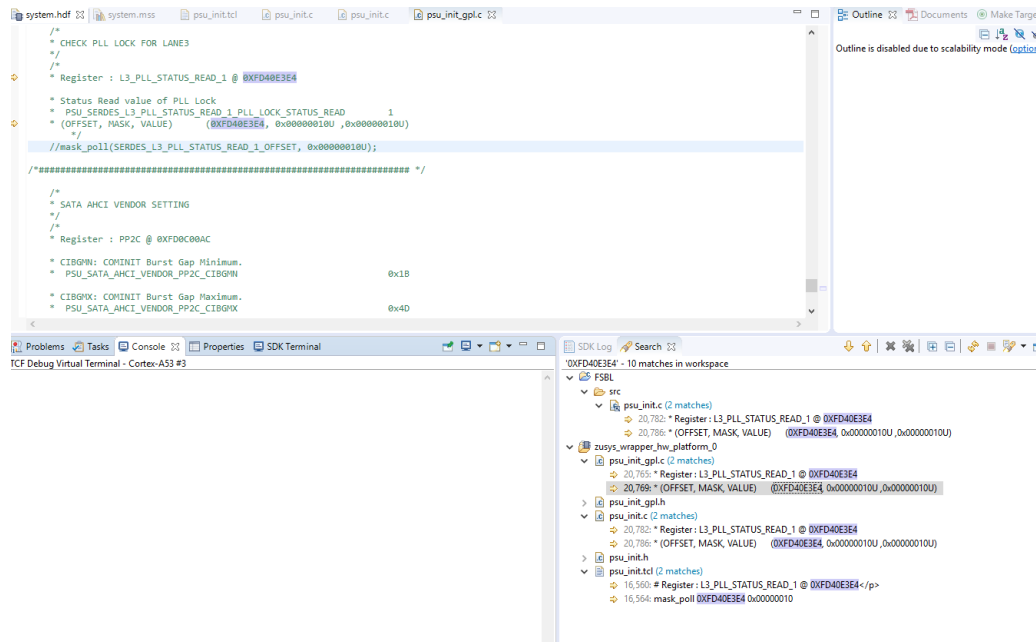
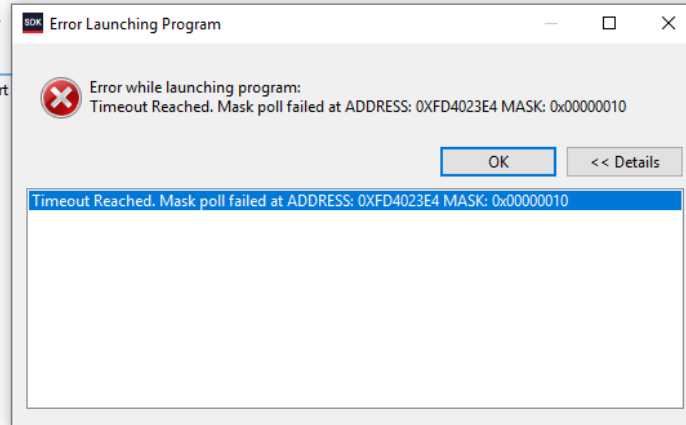
Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and environment, such as standard input and output, profiling, abort and exit.

Documentation: [standalone v6.7](#)

Peripheral Drivers

Drivers present in the Board Support

psu_acpu_gic scugic
psu_adma_0 zdma
psu_adma_1 zdma
psu_adma_2 zdma
psu_adma_3 zdma
psu_adma_4 zdma
psu_adma_5 zdma
psu_adma_6 zdma
psu_adma_7 zdma
psu_afi_0 generic
psu_afi_1 generic
psu_afi_2 generic
psu_afi_3 generic



```

Xilinx Zynq MP First Stage Boot Loader <TE modified>
Release 2018.2 Jan 9 2020 - 09:28:41
Reset Mode = System Reset
Platform: Silicon (4.0), Cluster ID 0x80000000
Running on A53-0 (64-bit) Processor, Device Name: XCZU15EG
-----
TE0808 Board Initialisation
Si534x Init Function
Si534x Init Complete
PCIe Reset Complete
-----
Processor Initialization Done
===== In Stage 2 =====
QSPI 32 bit Boot Mode
QSPI is in Dual Parallel connection
QSPI is using 4 bit bus
FlashID=0x20 0xBB 0x20
MICRON 512M Bits
Multiboot Reg : 0x4000
QSPI Reading Src 0x20000000, Dest FFFF1C40, Length EC0
XFSBL_ERROR_QSPI_LENGTH
Device Copy Failed
Boot Device Initialization failed 0x19
===== In Stage Err =====
Fshl Error Status: 0x0

```

Using Lwip sometimes I get the following:

```

-----lwIP TCP echo server -----
TCP packets sent to port 6001 will be echoed back
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation

```

Or

```
-----lwIP TCP echo server -----  
TCP packets sent to port 6001 will be echoed back  
Start PHY autonegotiation  
Waiting for PHY to complete autonegotiation.  
autonegotiation complete  
link speed for phy address 0: 1000  
DHCP Timeout  
Configuring default IP of 192.168.1.10  
Board IP: 192.168.1.10  
Netmask : 255.255.255.0  
Gateway : 192.168.1.1  
TCP echo server started @ port 7
```

Even when I remove the SFP connector from the cage. !!!!