

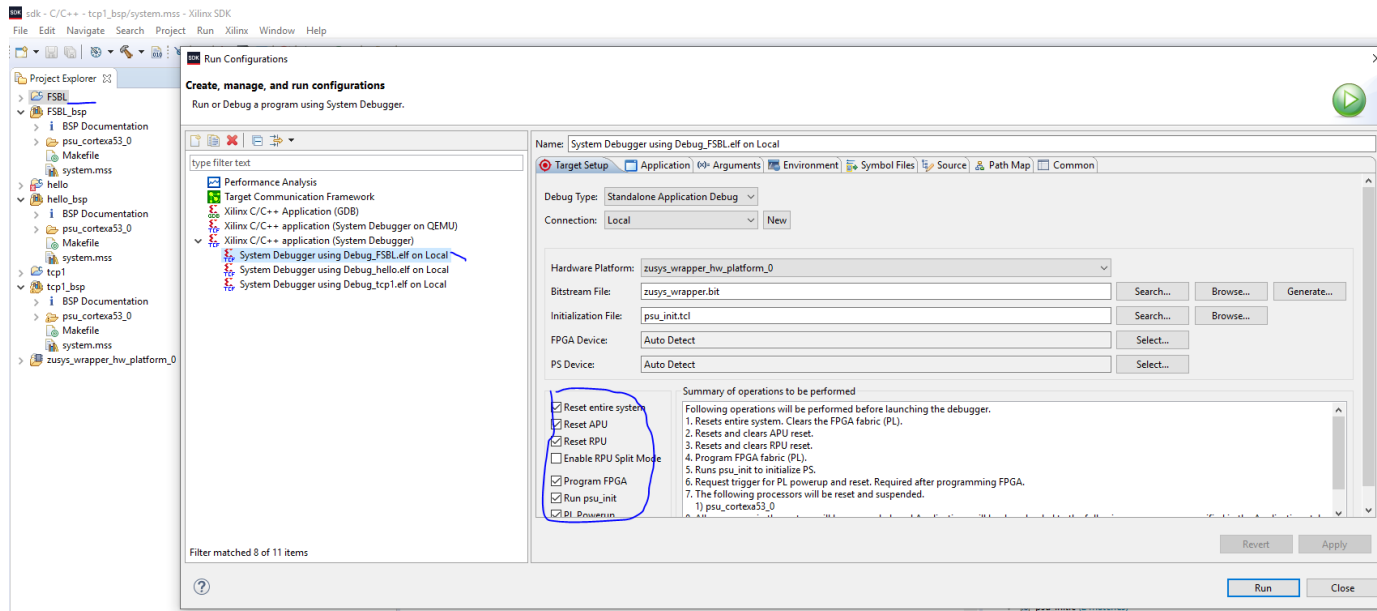
SFP with Ethernet

Thursday, January 9, 2020

2:15 PM

For testing SFP with Ethernet I do the following:

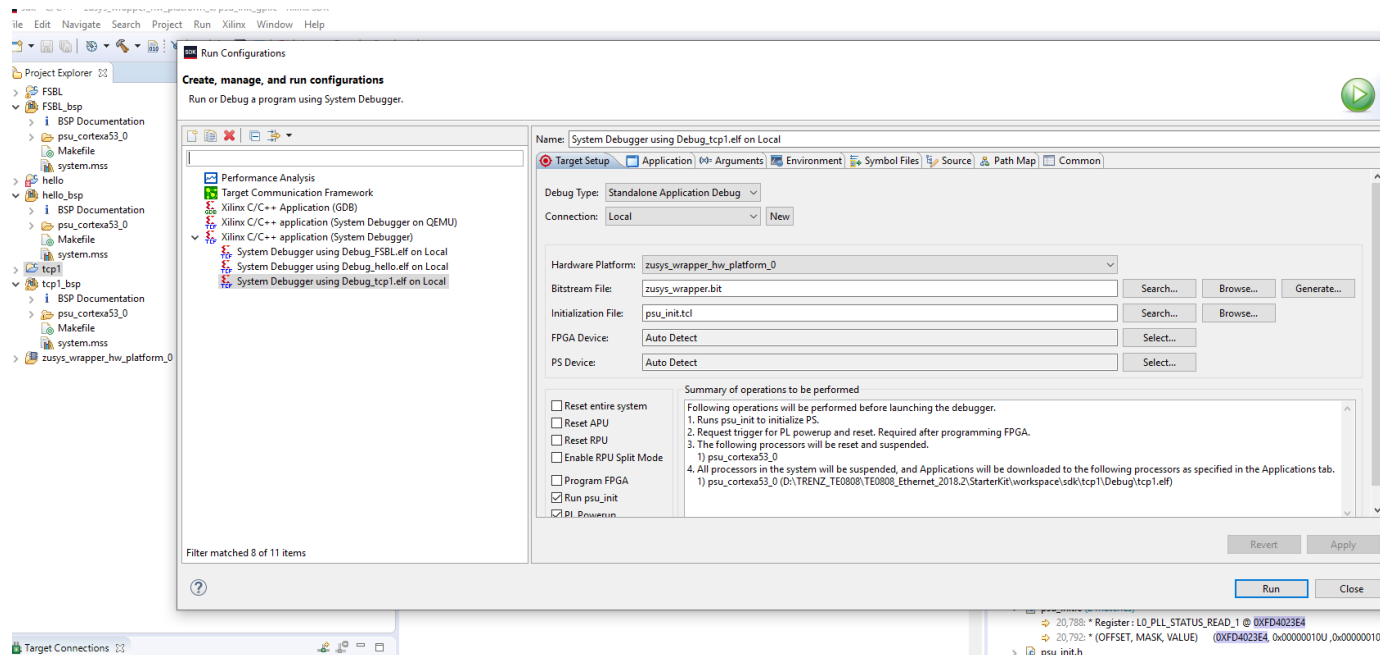
1. Open Vivado Hardware Manager
2. Program the FSBL using SDK



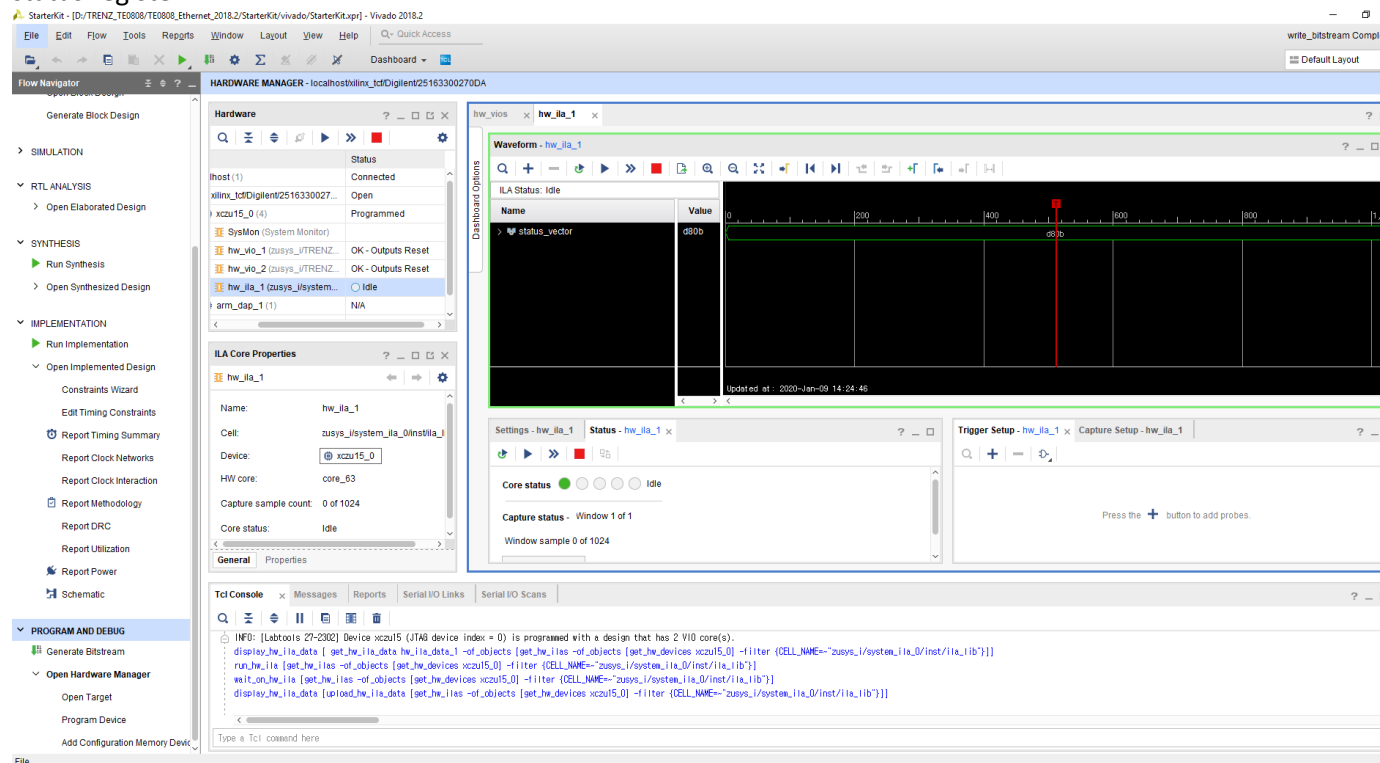
If you get the following error --> comment the dedicated lines:

Error while launching program: Timeout Reached. Mask poll failed at ADDRESS: 0XFD4023E4
MASK: 0x00000010

3. Program the lwip example using SDK.



4. After programming is done ---> refresh the Vivado Hardware Manager and check the value of the status register.



5. On the terminal you must see the PHYSICAL address you gave to the 1G/2.5G PCA PMA IP block.

```

Xilinx Zynq MP First Stage Boot Loader (TE modified)
Release 2018.2 Jan 9 2020 - 12:02:01
Reset Mode: System Reset
Platform: Silicon (4.0), Cluster ID 0x80000000
Running on A53-0 (64-bit) Processor, Device Name: XCZU15EG

-----
TE0808 Board Initialisation
Si534x Init Function
Si534x Init Complete
PCIe Reset Complete

-----
Processor Initialization Done
===== In Stage 2 =====
QSPI 32 bit Boot Mode
QSPI is in Dual Parallel connection
QSPI is using 4 bit bus
FlashID=0x20 0xBB 0x20
MICRON 512M Bits
Multiboot Reg : 0x4000
QSPI Reading Src 0x20000000, Dest FFFF1C40, Length EC0
XFSBL_ERROR_QSPI_LENGTH
Device Copy Failed
Boot Device Initialization failed 0x19
===== In Stage Err =====
Fshl Error Status: 0x0

-----lwIP TCP echo server -----
TCP packets sent to port 6001 will be echoed back
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
link speed for phy address 9: 1000
DHCP Timeout
Configuring default IP of 192.168.1.10
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
TCP echo server started @ port 7

```

6. gg